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MS Appeal Brief- Patents **Commissioner for Patents** **U.S. Patent and Trademark Office**	(571) 273-8300	(571) 272-8634

FROM: Thomas Chan
Reg. No. 51,543

DATE: September 19, 2007

Number of pages with cover page:	**25**	

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Comments:

Official Filing

Docket No.: 188122001700
Art Unit: 2128
Examiner: D. Silver
U.S. Patent Application Serial No.: 10/713,729
Filing Date: November 13, 2003
Inventor(s): Bruce W. MCGAUGHY et al.
Title: SYSTEM AND METHOD FOR DYNAMICALLY COMPRESSING CIRCUIT COMPONENTS DURING SIMULATION

Papers enclosed herewith:

1. Transmittal Form (1 page)
2. Fee Transmittal + duplicate for fee processing (2 pages)
3. Appeal Brief (21 pages)

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	24

Application Number	10/713,729
Filing Date	November 13, 2003
First Named Inventor	Bruce W. MCGAUGHY
Art Unit	2128
Examiner Name	D. Silver
Attorney Docket Number	188122001700

ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form + duplicate for fee processing (2 pages)
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC (21 pages) **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	MORRISON & FOERSTER LLP (Customer No. 25226)		
Signature			
Printed name	Thomas Chan		
Date	September 19, 2007	Reg. No.	51,543

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Dated: September 19, 2007 Signature: _____ (Carol Diez)

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FEE TRANSMITTAL
For FY 2007

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/713,729
Filing Date	November 13, 2003
First Named Inventor	Bruce W. MCGAUGHY
Examiner Name	D. Silver
Art Unit	2128
Attorney Docket No.	188122001700

METHOD OF PAYMENT (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	0
Design	200	100	100	50	130	65	0
Plant	200	100	300	150	160	80	0
Reissue	300	150	500	250	600	300	0
Provisional	200	100	0	0	0	0	0

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
24	- 24 = 0	x 50.00	= 0.00

HP = highest number of total claims paid for, if greater than 20.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
360.00	0.00

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
3	- 3 = 0	x 200.00	= 0.00

HP = highest number of independent claims paid for, if greater than 3.

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01 FC:1402 500.00 OA

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ /50 =	_____ (round up to a whole number) x	_____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	51,543	Telephone	(650) 813-5616
Name (Print/Type)	Thomas Chan			Date	September 19, 2007

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Dated: September 19, 2007 Signature: _____ (Carol DE2)

Docket No.: 188122001700
Client Reference No.: CAD-03-091
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Bruce W. MCGAUGHY et al.

Application No.: 10/713,729 Confirmation No.: 2684

Filed: November 13, 2003 Art Unit: 2128

For: SYSTEM AND METHOD FOR DYNAMICALLY COMPRESSING CIRCUIT COMPONENTS DURING SIMULATION Examiner: D. Silver

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on July 19, 2007, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter

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VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Claims
IX. Evidence
X. Related Proceedings
Appendix A Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Cadence Design Systems, Inc., a corporation duly organized under and pursuant to the laws of Delaware, with a principal place of business at 2655 Seely Avenue, Bldg. 5, San Jose, CA 95134.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 24 claims pending in application.

In the Advisory Action, the Examiner has rejected claims 1-23. **Applicants respectfully request the Examiner to clarify the status of claim 24.**

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B. Current Status of Claims

1. Claims canceled: 0

2. Claims withdrawn from consideration but not canceled: 0

3. Claims pending: 1-24

4. Claims allowed: 0

5. Claims rejected: 1-23

C. Claims On Appeal

The claims on appeal are claims 1-24.

IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final Rejection on July 19, 2007. The Examiner responded to the Amendment After Final Rejection in an Advisory Action mailed August 8, 2007. In the Advisory Action, the Examiner indicated that Applicants' proposed amendments and presented arguments do overcome the 101 rejections. However, the Examiner indicated that Applicants' arguments relating to the double patenting and 102(e) rejections have been considered but do not place the application in condition for allowance because these rejections have been previously addressed in the Final Office Action dated 4/19/2007.

Accordingly, the claims in Appendix A do incorporate the amendments indicated in the paper filed by Applicants on July 19, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed inventions are directed to a system and method for dynamically compressing circuit components represented in a hierarchical data structure during simulation. According to an embodiment of the present invention, a method of simulating a circuit having a hierarchical data structure comprises selecting a group of leaf circuits from a first branch and a

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second branch of the hierarchical data structure for simulation, representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior, creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit, where the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits, simulating the group of leaf circuits in accordance with the first port connectivity interface, and storing simulation results of the group of leaf circuits in a memory device.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-24 should be rejected on the ground of nonstatutory double patenting over claims 1-18 of U.S. Patent No. 7,024,652 (hereinafter the '652 patent).

B. Whether claims 1-24 should be rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,577,992 (hereinafter the '992 patent).

VII. ARGUMENT

Claims 1-24 were rejected by the Examiner in the Final Office Action mailed on April 19, 2007. Applicants respectfully request reversal of the rejection of these claims in view of the following remarks.

A. The Double Patenting Rejection Should Be Withdrawn

1) The matrix claimed in the '652 patent cannot function as the port connectivity interface and does not have the structure of the port connectivity interface of the pending claims

Applicants has presented in the responses to the Office Actions that pending claims requires the **port connectivity interface** be created dynamically for the group of leaf circuits in response to the merged leaf circuit, where the merged leaf circuit is created in response to two or more leaf circuits having a substantially same isomorphic behavior, and the **port connectivity**

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interface communicates changes in signal conditions among the group of leaf circuits. Applicants respectfully submit that the '652 patent does not claim any of these elements.

The response by the Examiner on this issue is shown in section 14 (page 5) of the final Office Action. The Examiner relies on the matrix in the '652 patent that allegedly represents the port connectivity interface of the pending claims. In particular, the Examiner states that:

> the matrix is a "set of equations that represent the one or more leaf circuits contained in the group circuit. The group circuit matrix also contains solution vectors corresponding to the set of equations." **(col: 9 line 51-56)**. Further, "[a] group circuit is associated with a group solver for solving the matrix associated with the group circuit. A group circuit also includes references to an event, which supports adding and deleting circuits in the group **dynamically** in response to **changes in signal conditions during simulation." (col: 14 line:36-49)**

Applicants respectfully submit that although a matrix may be used to represent one or more leaf circuits contained in a group circuit, it does not mean the matrix contains other features or functions in a group circuit. **After all, it is just a set of linear differential equations!** Person skilled in the art would understand that the set of linear equations do not contain **references** (such as pointers in computer programming) to access an **event. The Examiner has not shown the link between the matrix and the references to an event.** Therefore, the Examiner has not shown the **matrix** is capable of communicating changes in signal conditions among the group of leaf circuits as required in the pending claims for the port connectivity interface. In addition, the Examiner has not shown the structure of matrix that matches the structure of the port connectivity interface in the pending claims (see claims 4 for example).

In section 14.2, the Examiner indicates certain descriptions of the '652 patent that discloses the claimed isomorphic partitioning. Applicants respectfully submit that this statement is irrelevant because the '652 patent does not claim the isomorphic behavior of the leaf circuits.

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2) The Office Actions and Advisory Action have not addressed the differences between the electrical properties of Isomorphic Behavior and Strength of Coupling between two circuit components

In the responses to the First Office Action and the Final Office Action, Applications have explained the differences between the claim terms "isomorphic behavior" in the pending application versus the "strength of coupling" in the '652 patent. In particular, **the isomorphic behavior concerns about electrical properties of the leaf circuits**, such as the input/output signals, external loads, internal topologies, and internal states of the leaf circuits (see claims 2 and 7 for example). **The strength of coupling of leaf circuits concerns about the electrical properties of connection between leaf circuits**, which may vary from strong (when the connection is in on) to week (when the connection is off). Applicants invite the board and the Examiner to review the detailed explanations and examples provided in the previous responses to the Office Actions.

Based on the reasons presented above, Applicants respectfully request the double patenting rejection be withdrawn.

B. The Rejection under 35 U.S.C.102 (e) Rejection Should be Withdrawn

1) The approach of the '992 patent has been described in the background section of the current application

In the responses to the Office Actions, Applicants have presented that that one of the key differences between the current invention and the '992 patent lies in how dynamic information among the circuit components under simulation is communicated and what data structure are used for communicating such dynamic information during a transient simulation. It is known in the art that during a simulation, the simulator needs to keep track of port connectivity information of the circuit components. It is also known that during a simulation, the circuit components will go through different dynamic states. So the issue is not whether the port connectivity information or dynamic states exist or not, but how are they stored or used by the simulator.

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The '992 patent describes a method of storing dynamic voltage states within each instance of a subcircuit, and such dynamic voltage states information are accessed via pointers of the instance circuits (see Figure 2D of the '992 patent). All the circuit instances are connected hierarchically in a static circuit storage (see column 3, lines 56-67, and Figure 2 of the '992 patent). This approach is described in the background section of the pending application (see Figure 6 and its corresponding description).

The '992 patent chooses to store such information in the static database while the current invention uses a newly created dynamic data structure called the port connectivity interface for storing and communicating such dynamic information during simulation. However, there is major design tradeoffs involved in each implementation approach. The pending application describes the approach of the '992 patent in Figure 6 and its corresponding paragraphs [0018] – [0020] in the background section of the specification. In particular, the '992 patent employs pointers to pass such dynamic information through the subcircuit instances (See Figure 2C of the '992 patent.) Therefore, to pass information from one subcircuit to the next subcircuit in a different hierarchical branch, such as from subcircuit 620 to subcircuit 622 as shown in Figure 6 of the pending application, the simulator of the '992 patent would have to made multiple program calls (via the pointers). As indicated in the background section of the pending application, the problem with the method taught by '992 patent is that the dynamic information needs to traverse many levels of the hierarchical data structure before reaching its destination. At each hierarchical level, information needs to be synchronized before it may be transmitted to the next level, which the '992 patent are totally silent about these design issues. Therefore, the method of passing information through the hierarchies and synchronizing at each intermediate level, as taught by the '992 patent, would result in lower simulation performance.

To address the distinction between the '992 patent and the pending application, **Applicants respectfully request the Examiner to respond to the following questions in the Examiner's Answer regarding the '992 patent**: 1) How changes in signal conditions among the leaf circuits are communicated between each other (relevant to claim 1)? 2) What data structure is used to facilitate this communication (relevant to claim 1)? 3) What are the elements of this data structure (relevant to claim 4)? 4) What happens when two or more leaf circuits have a substantially

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same isomorphic behavior (relevant to claims 1 and 2)? 5) What happens when two or more leaf circuits demonstrate substantially different isomorphic behavior (relevant to claims 5 and 6)?

2) The '992 patent does not disclose at least the port connectivity interface and therefore the creation of the port connectivity interface in response to isomorphic behavior of the leaf circuits

The '992 patent does not describe the port connectivity interface (a dynamically created data structure) for communicating changes in signal conditions among the group of leaf circuits selected for simulation. The structure and use of the port connectivity interface is described in Figure 12B and Figure 8B and their corresponding descriptions of the pending application.

The response by the Examiner on this issue is shown in section 23 (page 8) of the final Office Action. In particular, the Examiner states that:

> Attention is drawn to **(col:3 line: 56-67)**, which discloses dynamic data structures (holds the dynamic voltages states) used in conjunction with the static storage. Therefore, when taken as a whole, Tcherniaev indeed has a "dynamic data structure", which directly correlates to the port connectivity interface claimed in the Instant Application.

After reviewing the paragraph cited by the Examiner in detail, Applicants respectfully submit that although the term "dynamic voltage states" has been mentioned a few times, the only storage element mentioned in the paragraph is the **static circuit storage**, which does not disclose the **dynamically** created data structure **port connectivity interface** for storing and handling dynamic information created during the simulation. The lack of disclosure of the port connectivity interface is consistent with the teachings of the '992 patent. For example, the '992 patent teaches that "[T]he static storage may therefore store the matrix structure. As described above, the static subcircuit storage 212 may further include a subcircuit definition 217 that defines the subcircuit topology. In addition, the static subcircuit storage 212 may provide element definitions 219 associated with the subcircuit definition 217." (See the '992 patent, column 9, lines 50-55, emphasis added.) The '992 patent also teaches that "[I]t is important to note that the circuit

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simulation is advantageously accomplished by traversing a hierarchical data structure such as that illustrated in FIG. 2A without flattening the hierarchical data structure." (See the '992 patent, column 10, lines 7-10, emphasis added.) The '992 patent further states that "[I]n addition to sharing an equivalent circuit structure and therefore static subcircuit storage, two subcircuit instances may have an equivalent dynamic voltage state obtained during transient simulation. As shown in FIG.2C, multiple instances 224, 226, 228 of the same subcircuit definition may share the same static subcircuit storage 212 as described above." The '992 patent further teaches that "one or more pointers ... may be used to permit both the first instance 224 and the third instance 228 to share this dynamic voltage state." (See the '992 patent, column 10, lines 17-33, emphasis added.) Applicants also note that column 14 lines 39-54 and column 16 line 35 to column 17 line 47 of the '992 patent teaches updating rate of change in node voltage, again by using pointers to traverse the hierarchical data structure. It is clear that the '992 patent teaches storing dynamic simulation information in the static subcircuit storage and using pointers to traverse the hierarchical data structure for passing dynamic information among subcircuits under simulation. The '992 patent is totally silent about the design issues, such as multiple program calls and synchronization between hierarchies, associated with its approach. No dynamic data structure, such as the port connectivity interface, is created by the '992 patent in response to the isomorphic behavior of the group of leaf circuits under simulation. The present invention addresses these design issues by using the port connectivity interface to facilitate communication of dynamic information among circuit components under simulation.

For at least the reasons presented above, Applicants respectfully submit that the '992 patent does not disclose each and every element of the independent claims 1, 9, and 17. Applicants also assert that claims 2-8, 10-16, and 18-24, which variously depend from their independent claims, are allowable for at least the reason that they depend from allowable independent claims. Applicants respectfully request the rejection under 35 U.S.C. 102(e) be withdrawn.

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VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Applicant on July 19, 2007.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: September 19, 2007

Respectfully submitted,

By _____

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/713,729

Claim 1 (Previously presented): A method of simulating a circuit having a hierarchical data structure, comprising:

representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches;

selecting a group of leaf circuits from the first and second branches for simulation;

representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior;

creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit; wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits;

simulating the group of leaf circuits in accordance with the first port connectivity interface; and

storing simulation results of the group of leaf circuits in a memory device.

Claim 2 (Previously presented): The method of claim 1, wherein the substantially same isomorphic behavior comprises:

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a substantially same set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits;

a substantially same set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and

a substantially same set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals.

Claim 3 (Original): The method of claim 1, wherein the substantially same isomorphic behavior is monitored at the output ports of the leaf circuits and at the first port connectivity interface of the group of leaf circuits.

Claim 4 (Original): The method of claim 1, wherein the first port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits;

a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits;

a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

Claim 5 (Previously presented): The method of claim 1, further comprising:

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splitting the merged leaf circuits into two or more individual leaf circuits in response to the two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors;

creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits; wherein the second port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and

simulating the group of leaf circuits in accordance with the second port connectivity interface.

Claim 6 (Previously presented): The method of claim 5, wherein substantially different isomorphic behaviors include one or more elements selected from the group consisting of:

a substantially different set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits;

a substantially different set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and

a substantially different set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals.

Claim 7 (Original): The method of claim 5, wherein the substantially different isomorphic behaviors are monitored at the output ports of the leaf circuits and at the second port connectivity interface of the group.

Claim 8 (Original): The method of claim 5, wherein the second port connectivity interface comprises:

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a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits;

a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits;

a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

Claim 9 (Previously presented): A system for simulating a circuit having a hierarchical data structure, comprising:

at least one processing unit for executing computer programs;

a user interface for performing at least one of the functions selected from the group consisting of entering a netlist representation of the circuit, viewing representations of the circuit on a display, and observing simulation results of the circuit;

a memory for storing static and dynamic information of the circuit;

a simulator module for simulating a circuit having a hierarchical data structure, wherein the simulator module is used in conjunction with at least a processing unit, a user interface and a memory, and the simulator module includes:

means for representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are

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interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches;

means for selecting a group of leaf circuits from the first and second branches for simulation;

means for representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior;

means for creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit; wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and

means for simulating the group of leaf circuits in accordance with the first port connectivity interface.

Claim 10 (Previously presented): The system of claim 9, wherein the substantially same isomorphic behavior comprises:

a substantially same set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits;

a substantially same set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and

a substantially same set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals.

Claim 11 (Original): The system of claim 9, wherein the substantially same isomorphic behavior is monitored at the output ports of the leaf circuits and at the first port connectivity interface of the group of leaf circuits.

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Claim 12 (Original): The system of claim 9, wherein the first port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits;

a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits;

a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

Claim 13 (Previously presented): The system of claim 9, further comprising:

splitting the merged leaf circuits into two or more individual leaf circuits in response to the two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors;

creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits; wherein the second port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and

simulating the group of leaf circuits in accordance with the second port connectivity interface.

Claim 14 (Previously presented): The system of claim 13, wherein substantially different isomorphic behaviors include one or more elements selected from the group consisting of:

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a substantially different set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits;

a substantially different set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and

a substantially different set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals.

Claim 15 (Original): The system of claim 13, wherein the substantially different isomorphic behaviors are monitored at the output ports of the leaf circuits and at the second port connectivity interface of the group.

Claim 16 (Original): The system of claim 13, wherein the second port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits;

a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits;

a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

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Claim 17 (Previously presented): A computer program product, comprising a medium storing computer programs for executing by one or more computer systems, the computer program comprising:

a simulator module for simulating a circuit having a hierarchical data structure, wherein the simulator module is used in conjunction with at least a processing unit, a user interface and a memory, and the simulator module includes one or more computer programs containing instructions for:

representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph; the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits; wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches;

selecting a group of leaf circuits from the first and second branches for simulation;

representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior;

creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit; wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits;

simulating the group of leaf circuits in accordance with the first port connectivity interface; and

storing simulation results of the group of leaf circuits in a memory device.

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Claim 18 (Previously presented): The computer program product of claim 17, wherein the substantially same isomorphic behavior comprises:

a substantially same set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits;

a substantially same set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and

a substantially same set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals.

Claim 19 (Original): The computer program product of claim 17, wherein the substantially same isomorphic behavior is monitored at the output ports of the leaf circuits and at the first port connectivity interface of the group.

Claim 20 (Original): The computer program product of claim 17, wherein the first port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits;

a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits;

a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

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Claim 21 (Previously presented): The computer program product of claim 17, further comprising instructions for:

splitting the merged leaf circuits into two or more individual leaf circuits in response to the two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors;

creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits; wherein the second port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and

simulating the group of leaf circuits in accordance with the second port connectivity interface.

Claim 22 (Previously presented): The computer program product of claim 21, wherein substantially different isomorphic behaviors include one or more elements selected from the group consisting of:

a substantially different set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits;

a substantially different set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and

a substantially different set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals.

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Claim 23 (Original): The computer program product of claim 21, wherein the substantially different isomorphic behaviors are monitored at the output ports of the leaf circuits and at the second port connectivity interface of the group.

Claim 24 (Original): The computer program product of claim 21, wherein the second port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits;

a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits;

a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

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